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AUG 2000 Technology Collaboration and Licensing

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DISCLOSURE AND RECORD OF INVENTION FORM

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Arizona State University
Office of Technology Collaborations & Licensing

ASU Disclosure # M1-008

1. Short descriptive title of the invention.

PROGRAMMABLE METALLIZATION CELL WITH FLOATING ELECTRODE

CIRCUMSTANCES OF THE INVENTION

2. List the funding source(s) for the project under which this invention was made. Identify by contract or grant number as well as Area/Org No. and name of the Principal Investigator.

Funding Source / Sponsor	Contract or Grant Number	Area/Org No.	Principal Investigator
AXON TECHNOLOGIES	TCL 00-1048	DWT 0099	M.N. KOZICKI

3. For any "Inventor" named on page 3 who is not employed full-time by Arizona State University, please identify their employers, the percent of salary time funded by such other employer, the nature of the other employment (such as research, teaching or clinical duties), AND WHERE THEIR INVENTIVE CONTRIBUTION WAS MADE.

4. When did you first conceive this invention? [redacted]

5. What is the date of the first written record (notebook, letter, proposal, drawing, etc.) of this invention? Identify the document, page numbers involved, and location of the document (please attach copies, if possible).

LABORATORY NOTEBOOK, DR. MICHAEL KOZICKI (6/2/00)

6. When did you first successfully test this invention? 6/23/00

7. Identify any references, patent applications, or other publications of which you are aware and which you believe to be pertinent to this invention. Please attach a copy of each of these references, if available.

SEE PATENT TREE

8. If any proprietary material (e.g., cell line, antibody, plasmid, computer software, or chemical compound) obtained from utside y ur lab ratory was used t develop this invention under a written transfer agreement (other than a n rmal purchasing agreement), please attach a c py of that agreement if available. If it is n t available, please let us kn w if the document exists, and, possibly, where it may be.

DISCLOSURE & PUBLICATION PLANS (EXTREMELY IMPORTANT)

Public disclosure affects patent rights – Please answer diligently

9. **If you have disclosed this invention to non-ASU personnel (including research sponsor) then indicate when, under what circumstances, and to whom.** NO PUBLIC DISCLOSURE

   a. **orally:** —

   b. **in writing:** —

   c. **by actual use, demonstration, or posters:** —

10. **Have you submitted or do you plan to submit a report, abstract, paper, poster, or thesis relating to this invention for publication, for presentation at a conference, or to a research sponsor?**

    YES ☐ **NO** ☒

    If yes, give details, including the <u>actual or planned date of submission as well as expected time to acceptance</u>. If a manuscript has been accepted, give the anticipated publication date. <u>Append a copy of the latest draft manuscript available.</u>

THE INVENTION ITSELF AND ITS UTILITY

11. A. **Brief summary of the invention:**
    <u>Include novel features and advantages. Describe possible commercial applications</u>

    SEE ATTACHED SHEETS

    B. **Detailed description of the invention: <u>Attach as many additional sheets as necessary.</u>**

    SEE ATTACHED SHEETS

12. **List companies you believe might be interested in using, developing or marketing this inventi n.**

    AXON TECHNOLOGIES CORPORATION

THIS INVENTION DISCLOSURE W[illegible] NOT BE PROCESSED UNLESS THIS PORT[illegible] IS FILLED OUT COMPLETELY

13. **Signatures, Names and addresses of Inventors**

The undersigned agree to comply with ABOR policies on intellectual property and to execute suitable assignments of title if and when asked to do so.

Signature [illegible] Date [illegible]	Signature [illegible] Date [illegible]
Print Name [illegible] Social Security Number [illegible]	Print Name [illegible] Social Security Number [illegible]
Position [illegible] Dept. [illegible]	Position [illegible] Dept. [illegible]
Arizona State University	Arizona State University
Campus (Address if non-ASU) Rm & Bldg [illegible]	Campus (Address if non-ASU) Rm & Bldg [illegible]
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City / State / Zip Mail Code [illegible]	City / State / Zip Mail Code [illegible]
Telephone [illegible] FAX [illegible]	Telephone (602) [illegible] FAX (602) [illegible]
E-mail Address [illegible]	E-mail Address [illegible]
Home Address [illegible]	Home Address [illegible]
City / State / Zip [illegible]	City / State / Zip Tempe AZ [illegible]
Home telephone [illegible]	Home telephone [illegible]
Citizen of [illegible]	Citizen of Korea
Signature Date	Signature Date
Print Name Social Security Number	Print Name Social Security Number
Position Dept.	Position Dept.
Campus (Address if non-ASU) Rm & Bldg	Campus (Address if non-ASU) Rm & Bldg
City / State / Zip Mail Code	City / State / Zip Mail Code
Telephone FAX	Telephone FAX
E-mail Address	E-mail Address
Home Address	Home Address
City / State / Zip	City / State / Zip
Home telephone	Home telephone
Citizen of	Citizen of

Lower oxidizable layer – e.g. silver (required only if lower electrode is non-silver)
Solid solution 1 – e.g. silver in germanium selenide
Floating electrode – e.g. tungsten or other indifferent conductor
Solid solution 2 – e.g. silver in germanium selenide
Upper oxidizable layer – e.g. silver (required only if upper electrode is non-silver)
Upper electrode – e.g. silver or indifferent conductor

The horizontal variant would involve the same electrode options but deposited in a coplanar fashion on the surface of the solid solution such that the floating electrode is placed between the other two (connected) electrodes.

Basis of patent application and claims:

1. Use of a floating electrode in a PMC device or a derivative of such.
2. Use of oxidizable or indifferent electrode in this context.
3. Enhancement of data storage capabilty, allowing four easily read states (two bits) to be programmed in each cell of a PMC-like device.
4. Programming of the cell using polarity and current sequences.
5. Use of the device as a programmable anti-fuse element.
6. Formation of both horizontal and vertical variants of the device.

14. Technically Qualified Witnesses (Two Required)—invention disclosed to and understood by:

a) ______________________________________ ____________
Signature Date

____
Print Name

b) ______________________________________ ____________
Signature Date

____
Print Name

GROUP REVIEWED (KOZICKI, MITKOVA, YUN, ABERROUETTA)

NOTE: *When completed, the Disclosure and Record of Invention Form is an important legal document. Care should be taken in its preparation. Please refer to accompanying instructions. If you desire assistance, call the Office of Technology Collaborations & Licensing at 965-5670. Information contained in this document is maintained in confidence and normally will not be released to others except with attorney client privilege, to research sponsors as required by contract, under appropriate secrecy agreements, until a patent application is filed, the information is published, a determination not to file a patent application is made, or as may be required by law. The information contained should not be disclosed to others outside the University, except as described in section 9, without the approval of the ASU Office of Technology Collaborations & Licensing.*

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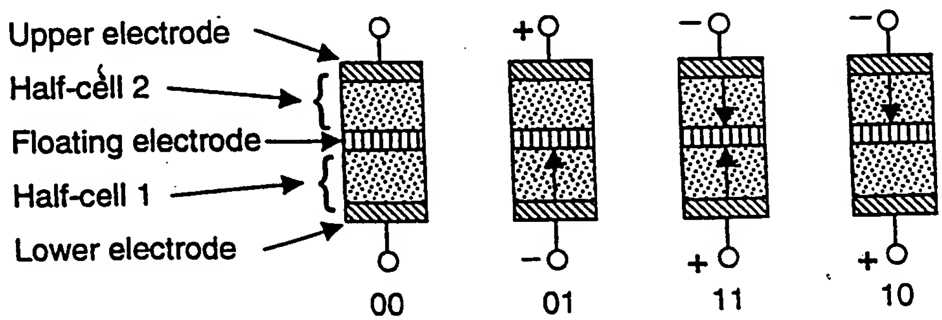
Bank One Building, 20 East University, Suite 201
Box 873511 Tempe, AZ 85287-3511

Effective 10/1/98

Programmable Metallization Cell with Fl ating El ctrode
Multi-state programmable microelectronic device

The Floating Electrode Programmable Metallization Cell (FEPMC) uses an unconnected (floating) electrode between layers of a solid solution. The FEPMC operates in a similar fashion to the two electrode (asymmetric) PMC device in that an electrodeposit is made to form on or in a solid solution by the application of a small potential. The low resistance metallic electrodeposit shorts out the high resistivity glass and can be subsequently removed by the application of a reverse bias. This is how information is stored in the PMC device. The unique structure of the FEPMC allows four distinct and easily programmed states, which can represent two bits of binary information, to be stored in a single device.

The FEPMC structure essentially has five layers; lower electrode, solid solution 1, floating electrode, solid solution 2, and upper electrode. (Note that although this description pertains to a vertical device, a horizontal structure is also possible with all three electrodes being deposited on the surface of a thin layer of the solid solution.) If the floating electrode is the same as the metal in solution and the lower and upper electrodes are indifferent, or *vice-versa*, the entire structure may be thought of as two back-to-back PMC devices with a common electrode. Each "half-cell" is a PMC device in its own right but the common electrode is only supplied with electrons or ions via the solid solution layers and not by any other external connection. The full structure is shown schematically in the figure below.



Considering first the case of a structure with an oxidizable floating electrode, e.g., silver. In the unprogrammed state, the half cells have geometry and solution dependent impedances of Z_1 for half-cell 1 and Z_2 for half-cell 2. Typically, the solution layer thicknesses will be chosen so that Z_1 and Z_2 are distinctly different. The overall impedance of the FEPMC structure will be given by Z_1 in series with Z_2 and this may be used to represent state 00. If a voltage is applied such that the upper electrode is positive with respect to the lower electrode and the magnitude is above that necessary to promote electrodeposition in half-cell 1, an electrodeposit will form from the lower electrode to the floating electrode as

shown by the arrow in the figure. Note that an electrodeposit will not grow in half-cell 2 as it is "reverse biased" and so will not support electrodeposition. The electrodeposit will change the impedance of half-cell 1 to Z_1', changing the overall impedance of the FEPMC and producing a value which may represent state 01. The current or charge limit will set the magnitude of the change and should be chosen sufficiently low so that it is possible to subsequently erase the electrodeposit with a reasonable current.

If the polarity is now reversed (with a similar low current level), most of the applied bias will be dropped across the high resistance solution of half-cell 2 rather than across half-cell 1, and so an electrodeposit will form from the top electrode to the floating electrode without dissolving the connection in half-cell 1, as shown in the figure. The impedance of half-cell 2 now becomes Z_2' and the overall impedance is Z_1' in series with Z_2'. This device impedance can be used to represent state 11.

Once both half-cells are shorted, either electrodeposit can be dissolved by applying a sufficient (reverse) bias across the appropriate half-cell. However, if the upper electrode is once again made negative with respect to the lower but using a higher current limit which allows sufficient reverse bias across half-cell 1, only this cell will be erased (see figure). Half-cell 1 will therefore return to Z_1 and the overall device impedance will be Z_1 in series with Z_2', representing state 10. The entire four state sequence is summarized in the table below.

Seq #	Polarity	Current limit	Z half-cell 1	Z half-cell 2	State/value
1	Sub-threshold	Zero	Z_1	Z_2	00
2	Upper + Lower –	Low	Z_1'	Z_2	01
3	Upper – Lower +	Low	Z_1'	Z_2'	11
4	Upper – Lower +	High	Z_1	Z_2'	10

It is possible to return to state 11 from state 10 simply by applying a low current limit bias to regrow the electrodeposit in half-cell 1 (upper +, lower -). From state 11, dissolving the electrodeposit in half-cell 2 by applying a high current limit bias such that the upper electrode is again positive with respect to the lower will take the device to state 01. Finally, if state 00 is now to be attained, a short current pulse must be applied to thermally dissolve the electrodeposit in half-cell 1. This can be done with the same polarity as the half-cell 1 write but with a current limit which is high enough to cause localized heating of the electrodeposit. This will increase the metal concentration in the half-cell but this excess metal can be removed electrically from the cell by plating it back onto the floating electrode (this will happen when half-cell 2 is written to, i.e., when the upper electrode is negative with respect to the lower). This sequence is summarized in the table below.

Seq #	Polarity	Current limit	Z half-cell 1	Z half-cell 2	State/value
4	Existing state	-	Z_1	Z_2'	10
5	Upper + Lower –	Low	Z_1'	Z_2'	11
6	Upper + Lower –	High	Z_1'	Z_2	01
7	Upper + Lower –	Thermal	Z_1	Z_2	00

Note that other sequences are possible (as are other definitions of the various states represented by the half-cell impedances). For example, it is possible to go from state 00 to either state 01 or state 10, depending on the write polarity chosen. Similarly, it is possible to go from state 11 to either state 10 or state 01. It is also possible to go from state 11 to state 00 by the application of a current pulse (in either direction) which is high and short enough to thermally dissolve the electrodeposits in both half-cells simultaneously.

In addition to storing information in digital form, the FEPMC can also be used as a noise-tolerant low energy anti-fuse element for use in field programmable gate arrays (FPGAs) and field configurable circuits and systems. Most physical anti-fuse technologies require large currents and voltages to make a permanent connection. The need for such high energy state-switching stimuli is generally considered to be somewhat beneficial as this reduces the likelihood of the anti-fuse accidentally forming a connection in electrically noisy situations. However, the use of high voltages and large currents on chip represent a significant problem as all components in the programming circuits have to be sized accordingly and the high energy consumption reduces battery life in portable systems.

The FEPMC represents a low energy anti-fuse solution which is relatively noise immune. The device can only be closed (fully shorted to the lowest impedance state) if a pulse of one polarity is followed by one of the opposite polarity. This eliminates the likelihood of switching due to unipolar voltage spikes, which are common in digital and mixed signal integrated circuits.

Two vertical configurations of the FEPMC are possible, both being formed by multi-layer deposition. Note that the vertical FEPMC can be fabricated so that it is entirely contained within a via in a dielectric layer. For an oxidizable floating electrode, the layer sequence would be as follows:

Lower electrode – e.g. tungsten or other indifferent conductor
Solid solution 1 – e.g. silver in germanium selenide
Floating electrode – e.g. silver
Solid solution 2 – e.g. silver in germanium selenide
Upper electrode – e.g. tungsten or other indifferent conductor

For a non-oxidizable floating electrode, the layer sequence would be as follows:

Lower electrode – e.g. silver or an indifferent conductor

Lower oxidizable layer – e.g. silver (required only if lower electrode is non-silver)
Solid solution 1 – e.g. silver in germanium selenide
Floating electrode – e.g. tungsten or other indifferent conductor
Solid solution 2 – e.g. silver in germanium selenide
Upper oxidizable layer – e.g. silver (required only if upper electrode is non-silver)
Upper electrode – e.g. silver or indifferent conductor

The horizontal variant would involve the same electrode options but deposited in a coplanar fashion on the surface of the solid solution such that the floating electrode is placed between the other two (connected) electrodes.

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